IN THE CLAIMS

Please **amend** claims 1, 9, 10, 17, 18, 26, 27, 35, 43, 45-48, 51, and 55 as provided in the Status of the Claims section, infra.. Additions to the amended claims are underlined and any deletions to the amended claims are presented either between double brackets or as struckthrough text.

Claims 1, 10, 17, 18, 27, 43, 48, and 55 have been amended to change the term "rounded off" to "rounded down" to be more precise. Accordingly, this claim is not a claim narrowing amendment as that term is understood according to the Festo decision. Indeed, the Applicants make this amendment without the intention to surrender the equivalents to which the claims are entitled.

Claims 9, 35, 47, 51, and 55 have been amended to change the term "Gaussian dispersion" to – Gaussian distribution --, which is the more correct English translation of the original Japanese text. No new matter has been added. Accordingly this is not a claim narrowing amendment as that term is understood according to the Festo decision.

Claims 26, and 45-47 have been amended to change the claim from which the amended claims depend. Accordingly this is not a claim narrowing amendment as that term is understood according to the Festo decision.

STATUS OF THE CLAIMS

1. (currently amended) An image processing apparatus, comprising:

a first signal processing circuit for applying gamma correction to an n-bit (n: a natural number) digital signal inputted as a video signal, and for converting the digital signal into an m-bit (m > n, m : a natural number) digital signal; and

a second signal processing circuit for adding a noise signal to the m-bit digital signal from said first signal processing circuit, and for outputting a Q-bit (Q: a natural number) digital signal obtained from rounding down[[~~off~~]] a less significant (m - Q) bit ($Q \leq n$) from the m-bit digital signal.

2. (Original) The image processing apparatus as set forth in Claim 1, wherein:

said first signal processing circuit includes bit converting means for converting the inputted n-bit digital signal into the m-bit digital signal in accordance with a pre-set value.

3. (Original) The image processing apparatus as set forth in Claim 2, wherein:

said bit converting means is a Look Up Table which outputs the m-bit digital signal that is the present value in accordance with the inputted n-bit digital signal.

4. (Original) The image processing apparatus as set forth in Claim 2, wherein:

said bit converting means is a calculating device for converting the n-bit digital signal into the m-bit (m > n) digital signal by numerical calculation.

5. (Original) The image processing apparatus as set forth in Claim 1, wherein:

said first signal processing circuit and said second signal processing circuit are provided for respective RGB colors.

6. (Original) The image processing apparatus as set forth in Claim 1, wherein:

an average value of a signal level of the noise signal is set to zero.

7. (Original) The image processing apparatus as set forth in Claim 1, wherein:

the noise signal is a random noise signal with no regularity in its cycle of amplitude.

8. (Original) The image processing apparatus as set forth in Claim 1, wherein:

the noise signal is obtained from, by using an arbitrary noise pattern table, switching a starting point of the noise pattern table per field or per noise pattern table.

9. (~~Original~~currently amended) The image processing apparatus as set forth in Claim 1, wherein:

a histogram of an amplitude of the noise signal shows Gaussian ~~dispersion~~distribution where zero amplitude of the noise signal is at the center.

10. (currently amended) An image processing apparatus, comprising:

a signal processing circuit for adding a noise signal to an inputted m-bit (m: a natural number) digital signal, and for outputting a Q-bit (Q: a natural number) digital signal obtained from rounding down[[~~off~~]] a less significant (m - Q) bit (Q < m) from the m-bit digital signal.

11. (Previously presented) An image display apparatus comprising:

an image processing apparatus as set forth in claim 1;

display means for displaying an image; and

driving means for driving the display means.

12. (Original) The image display apparatus as set forth in Claim 11, wherein:

said first signal processing circuit includes bit converting means for converting the inputted n-bit digital signal into the m-bit digital signal in accordance with a pre-set value.

13. (Original) The image display apparatus as set forth in Claim 12, wherein:

the pre-set value in said bit converting means is rewritable so that unevenness in properties of said driving means may be absorbed.

14. (Original) The image display apparatus as set forth in Claim 12, wherein:

the pre-set value in said bit converting means is rewritten in accordance with brightness in surroundings of said image display apparatus.

15. (Original) The image display apparatus as set forth in Claim 12, wherein:

the pre-set value in said bit converting means is rewritten in accordance with brightness of overall display image of said display means.

16. (Previously presented) An image display apparatus, comprising:

an image processing apparatus as set forth in claim 10.

17. (currently amended) An image processing apparatus, comprising:

a first signal processing circuit (a) for applying gamma correction to a digital video signal inputted therein, (b) for expanding a bit number of the digital video signal from n bit to m bit (m > n: n and m are natural numbers), and (c) for outputting the digital video signal; and

a second signal processing circuit (d) for adding a noise signal to the digital signal thus outputted from the first signal processing circuit, (e) for converting the number of the digital video signal from m bit to Q bit by rounding down[[~~off~~]] a less significant (m - Q) bit (Q ≤ n: Q is a natural number), and (f) for outputting the thus obtained digital video signal whose bit number is Q bit.

18. (currently amended) The image processing apparatus as set forth in Claim 17, wherein the second signal processing circuit includes:

a noise generating circuit for generating the noise signal;

an adding circuit for adding the noise signal thus generated by the noise generating circuit, into the digital video signal whose bit number is Q bit and that is supplied from the first signal processing circuit, and for outputting the digital video signal to which the noise is added;

a bit number converting circuit for converting the bit number of the digital video signal by rounding down[[~~off~~]] a less significant (m - Q) bit of the digital video signal whose bit number is m bit and to which the noise is added by the adding circuit.

19. (Previously presented) The image processing apparatus as set forth in Claim 18, wherein the noise generating circuit includes:

an address counter for outputting pixel addresses, the pixel addresses being incremented, pixel by pixel, in a horizontal direction and incremented, line by line, in a vertical direction,

a noise ROM for storing noise data enough for one screen, and for outputting the noise signal that is to be supplied per pixel, in accordance with the pixel addresses thus outputted from the address counter.

20. (Previously presented) An image display apparatus comprising:

an image processing apparatus as set forth in Claim 17;

display means for displaying an image; and

driving means for driving the display means.

21. (Previously presented) The image display apparatus asset forth in Claim 20, wherein the display means is a liquid crystal display.

22. (Previously presented) The image display apparatus as set forth in Claim 20, wherein the image processing apparatus is separately provided.

23. (Previously presented) The image display apparatus as set forth in Claim 20, wherein the first signal processing circuit is a lookup table for carrying out gamma correction, and wherein the image processing apparatus includes:

a sensor for detecting brightness in surroundings of the image display apparatus; and

a control circuit for rewriting a gamma value of the lookup table in accordance with output from the sensor.

24. (Previously presented) The image display apparatus as set forth in Claim 20, wherein the first signal processing circuit is a lookup table for carrying out gamma correction, and wherein the image processing apparatus includes:

an average value calculating circuit for calculating an average value of a signal level of a video signal; and

a control circuit for rewriting a gamma value of the lookup table in accordance with output from the average value calculating circuit.

25. (Previously presented) The image display apparatus as set forth in Claim 20, wherein the first signal processing circuit is a lookup table for carrying out gamma correction, and wherein the image processing apparatus includes:

an area judging circuit for judging an area to be displayed on the display means; and

a control circuit for rewriting a gamma value of the lookup table in accordance with output from the area judging circuit.

26. (currently amended) The image processing apparatus asset forth in Claim 11[[1]], wherein the display means is a liquid crystal display.

27. (currently amended) An image processing apparatus, comprising:

a first signal processing circuit for converting an n-bit (n: a natural number) digital signal inputted as a video signal, into an m-bit (m > n, m : a natural number) digital signal; and

a second signal processing circuit for adding a noise signal to the m-bit digital signal from said first signal processing circuit, and for outputting a Q-bit (Q: a natural number) digital signal obtained from rounding ~~off~~down a less significant (m - Q) bit (Q ≤ n) from the m-bit digital signal.

28. (previously presented) The image processing apparatus as set forth in Claim 27, wherein said first signal processing circuit includes bit converting means for converting the inputted n-bit digital signal into the m-bit digital signal in accordance with a pre-set value.

29. (previously presented) The image processing apparatus as set forth in Claim 28, wherein said bit converting means is a Look Up Table which outputs the m-bit digital signal that is the pre-set value in accordance with the inputted n-bit digital signal.

30. (previously presented) The image processing apparatus as set forth in Claim 28, wherein said bit converting means is a calculating device for converting the n-bit digital signal into the m-bit (m > n) digital signal by numerical calculation.

31. (previously presented) The image processing apparatus as set forth in Claim 27, wherein said first signal processing circuit and said second signal processing circuit are provided for respective RGB colors.

32. (previously presented) The image processing apparatus as set forth in Claim 27, wherein an average value of a signal level of the noise signal is set to zero.

33. (previously presented) The image processing apparatus as set forth in Claim 27, wherein the noise signal has no regularity in its cycle of amplitude.

34. (previously presented) The image processing apparatus as set forth in Claim 27, wherein the noise signal is obtained, by using an arbitrary noise pattern table, from switching a starting point of the noise pattern table per field or per noise pattern table.

35. (currently amended) The image processing apparatus as set forth in Claim 27, wherein a histogram of an amplitude of the noise signal shows Gaussian ~~dispersion~~distribution where zero amplitude of the noise signal is at the center.

36. (previously presented) The image processing apparatus as set forth in Claim 27, comprising a noise memory for storing the noise signal for one screen.

37. (previously presented) The image processing apparatus as set forth in Claim 27, comprising a noise memory for storing the noise signal per block that is smaller than one screen.

38. (previously presented) An image display apparatus comprising:
display means for displaying an image;
driving means for driving the display means; and

the image processing apparatus as set forth in Claim 27.

39. (previously presented) The image display apparatus as set forth in Claim 38, wherein said first signal processing circuit includes bit converting means for converting the inputted n-bit digital signal into the m-bit digital signal in accordance with a pre-set value.

40. (previously presented) The image display apparatus as set forth in Claim 39, wherein the pre-set value in said bit converting means is rewritable so that unevenness in properties of said driving means may be absorbed.

41. (previously presented) The image display apparatus as set forth in Claim 39, wherein the pre-set value in said bit converting means is rewritten in accordance with brightness in surroundings of said image display apparatus.

42. (previously presented) The image display apparatus as set forth in Claim 39, wherein the pre-set value in said bit converting means is rewritten in accordance with brightness of overall display image of said display means.

43. (currently amended) An image processing method comprising the steps of:

converting an n-bit (n: a natural number) digital signal inputted as a video signal, into an m-bit (m > n, m : a natural number) digital signal;

adding a noise signal to the m-bit digital signal; and

outputting a Q-bit (Q: a natural number) digital signal obtained from rounding ~~off~~down a less significant (m - Q) bit (Q ≤ n) from the m-bit digital signal.

44. (previously presented) The image processing method as set forth in Claim 43, wherein the inputted n-bit digital signal is converted into the m-bit digital signal in accordance with a pre-set value.

45. (currently amended) The image processing method as set forth in Claim 43 [[44]], wherein an average value of a signal level of the noise signal is set to zero.

46. (currently amended) The image processing method as set forth in Claim 43[[44]], wherein the noise signal has no regularity in its cycle of amplitude.

47. (currently amended) The image processing method as set forth in Claim 43[[44]], wherein a histogram of an amplitude of the noise signal shows Gaussian ~~dispersion~~distribution where zero amplitude of the noise signal is at the center.

48. (currently amended) An image processing method comprising the step of:

adding a noise signal to an m-bit digital signal (m: a natural number); and

subsequently outputting a Q-bit (Q: a natural number) digital signal obtained from rounding ~~off~~down a less significant (m - Q) bit (Q < m) from the m-bit digital signal.

49. (previously presented) The image processing method as set forth in Claim 48, wherein:

an average value of a signal level of the noise signal is set to zero.

50. (previously presented) The image processing method as set forth in Claim 48, wherein:

the noise signal has no regularity in its cycle of amplitude.

51. (currently amended) The image processing method as set forth in Claim 48, wherein:

a histogram of an amplitude of the noise signal shows Gaussian ~~dispersion~~distribution where zero amplitude of the noise signal is at the center.

52. (previously presented) The image processing apparatus as set forth in Claim 10, wherein:

an average value of a signal level of the noise signal is set to zero.

53. (previously presented) The image processing apparatus as set forth in Claim 10, wherein:

the noise signal has no regularity in its cycle of amplitude.

54. (previously presented) The image processing apparatus as set forth in Claim 10, wherein:

the noise signal is obtained from, by using an arbitrary noise pattern table, switching a starting point of the noise pattern table per field or per noise pattern table.

55. (currently amended) The image processing apparatus as set forth in Claim 10, wherein:

a histogram of an amplitude of the noise signal shows Gaussian ~~dispersion~~distribution where zero amplitude of the noise signal is at the center.

56. (New) An image processing apparatus, comprising:

a first signal processing circuit for processing with a predetermined operation an n-bit digital signal (n: natural number) inputted as a video signal to be converted into an m-bit digital signal (m > n, m: a natural number); and

a second signal processing circuit for adding a noise signal to the m-bit digital signal inputted from said first signal processing circuit, rounding down a less significant (M-Q) bit (Q ≤ n) from the m-bit digital signal having added thereto the noise signal, and outputting the resulting Q-bit digital signal.

57. (New) The imag e processing apparatus as set forth in claim 56, wherein;

said first signal processing circuit converts the n-bit digital signal as inputted into the m-bit digital signal according to display characteristics of display means of an image display apparatus provided with said image processing apparatus.

58. (New) The image processing apparatus as set forth in claim 56, wherein:

said first signal processing circuit converts the n-bit digital signal as inputted into the m-bit digital signal so as to absorb differences in performances of said driving means for driving display means of an image display apparatus provided with said image processing apparatus.

59. (New) The image processing apparatus as set forth in claim 56, wherein:

said first signal processing circuit converts the n-bit digital signal as inputted into the m-bit digital signal according to ambient brightness of an image display apparatus provided with said image processing apparatus.

60. (New) The imag e processing apparatus as set forth in claim 56, wherein:

said first signal processing circuit converts the n-bit digital signal as inputted into the m-bit digital signal according to brightness of overall display image on display means of an image display apparatus provided with said image processing apparatus.

61. (New) The imag e processing apparatus as set forth in claim 56, wherein:

said first signal processing circuit converts the n-bit digital signal as inputted into the m-bit digital signal according to an average level of an input signal to be inputted to an image display apparatus provided with said image processing apparatus.

62. (New) An image processing method comprising the steps of:

processing with a predetermined operation an n-bit digital signal (n: natural number) inputted as a video signal to be converted into an m-bit digital signal ($m > n$, m: a natural number); and

outputting a Q-bit digital signal obtained by adding a noise signal to the m-bit digital signal and rounding down a less significant (m-Q) bit ($Q \leq n$) from the m-bit digital signal having added thereto the noise signal.